What is claimed is:

1. A device for checking dependencies between instructions and issuing the instructions to an associated function unit based on the dependencies, said device comprising:

a dependency unit including a plurality of entries, each entry corresponding to an instruction slated for execution, elements of each entry indicating dependencies of the instruction on other instructions; and

connection lines for connecting elements of the entry that are located at a same position in the entries.

2. The device of claim 1 wherein said entries include registers that have elements indicating dependencies between instructions.

3. The device of claim 1 wherein said entries include circuitries that have a set of data holding places that indicates dependencies between the instructions.

4. The device of claim 1 wherein each said entry includes:

means for examining the elements of the entry to determine whether the instruction has dependencies on other instructions; and

means for making a request for issuing the instruction to be executed where the instruction is ready to issue.

5. The device of claim 1 further comprising a granting unit for generating to the entries in the dependency unit a signal for issuing instructions to the associated function unit.

6. The device of claim 5 wherein said granting unit is coupled with an entry located at n-th row in the dependency unit at n-th column element of the entry.

7. The device of claim 5 wherein said granting unit selects a predetermined number of instructions from instructions that make requests for issuing based on a selection criteria.

8. The device of claim 7 wherein said selection criteria includes a temporal criteria.

9. The device of claim 1 wherein said elements of each said entry are set where the instruction is dependent on another instruction to which the element of the entry corresponds.

10. The device of claim 1 further comprising means for manipulating elements of entries to a state indicating no dependencies, the resetting means being coupled with one of the connection lines.

11. The device of claim 5 further comprising means for manipulating elements of entries, the resetting means being triggered by the signal from the granting unit.

12. The device of claim 1 wherein each said element of each said entry is implemented using a memory cell.

13. A device for scheduling instructions with dependencies between the instructions, said device comprising:

a checking unit for checking dependencies between the instructions to generate dependency indication vectors having elements, said elements of a vector indicating dependencies of an instruction on other instructions;

an issuing unit for issuing the instructions to an associated function unit by implementing in hardware the dependency indication vectors, said hardware resetting the elements of the vectors to a state indicating no dependencies by connecting the elements of the vectors that are located at a same position in the vectors.

14. The device of claim 13 wherein said issuing unit implements the dependency indication vectors by using circuitries that have a set of data holding places that indicates dependencies between instructions.

15. The device of claim 14 wherein said circuitries includes registers that have elements indicating dependencies between instructions.

16. The device of claim 13 wherein said issuing unit implements the elements of the dependency indication vectors by using a memory cell that has a logical value of "0" or "1" to indicate dependency of an instruction on other instruction.

17. The device of claim 13 wherein said issuing unit transmits an issue signal of an instruction to instructions that depend on the issued instruction by connection lines,

connection lines connecting the elements of the vectors that are located at a same position in the vectors.

18. The device of claim 17 wherein said issuing unit comprises manipulating means for manipulating the elements of the dependency indication vector to a state indicating no dependencies.

19. The device of claim 18 wherein said manipulating means is implemented in hardware.

20. The device of claim 18 wherein said the manipulating means being coupled with one of connection lines connecting the elements of the vectors that are located at a same position in the vectors.

21. In a microprocessor architecture, a method for checking dependencies between instructions and issuing the instructions to an associated function unit based on the dependencies, the method comprising steps of:

checking dependencies between the instructions;

providing a scoreboard that indicates the dependencies between the instructions;

selecting a first set of instructions that are ready to issue based on the scoreboard indication; and

issuing a second set of instructions to the associated function unit, the second set of instructions being chosen from the first set of instructions.

22. The method of claim 21 further comprising the steps of:

broadcasting issuance of the second set of instructions to other instructions that depend on the second set of instruction; and

adjusting dependencies of other instructions on the second set of instructions based on the broadcast of the issuance of the second set of instructions.

23. The method of claim 22 wherein the dependencies of other instructions on the second set of instructions are adjusted substantially at a same of the issuance of the second set of instructions

24. The method of claim 21 further comprising the steps of:

selecting a third set of instructions that are ready to issue, the third set of instructions including instructions that has dependencies on the second set of instructions issued to the associated function unit.

25. The method of claim 24 further comprising the step of issuing the fourth set of instructions to the associated function unit in the following cycle, the fourth set of instructions being chosen from the third set of instructions.

26. The method of claim 21 wherein the first set of instructions are selected based on a predetermined number of instructions that can be executed at the same time in a microprocessor.

27. The method of claim 21 wherein the first set of instructions is selected based on a plurality of criteria including a temporal criteria.

28. The method of claim 21 wherein said step of providing a scoreboard comprising:
providing a entry for an instructions wherein each element of the entry corresponds to one of other instructions; and
setting elements of the entry corresponding to other instructions which the instruction depends on.

29. The method of claim 25 wherein said step of selecting a first set of instruction comprises:
examining the elements of the entry to determine whether the instruction has dependencies on other instructions; and
where an instruction is ready to issue, selecting the instruction.

30. A microprocessor for checking dependencies between instructions and scheduling the instructions based on the dependencies, said microprocessor comprising:
a checker for checking dependencies between the instructions;
a dependency unit for indicating the dependencies between the instructions; and
a granting unit for generating signals for issuing instructions to an associated function unit based on the indication of the dependency unit.

31. The microprocessor of claim 30 wherein said dependency unit comprises:
entries for representing instructions wherein said entries have elements that correspond to other instructions; and
wherein an element of a entry provided for an instruction is set where the instruction is dependent on one of other instructions which the element corresponds to.

32. The microprocessor of claim 31 wherein said dependency unit further comprises:

means for examining the elements of entries to determine whether the instruction has dependencies on other instructions; and

means for making a request for issuing the instruction to an associated function unit where the instruction is ready to issue.

33. The microprocessor of claim 32 wherein said granting unit grants signals for issuing instructions to a predetermined number of instructions from the instructions that make requests for issuing.

34. The microprocessor of claim 33 wherein said granting unit grants signals for issuing instructions to a predetermined number of instructions that can be executed at the same time in a microprocessor.

35. The microprocessor of claim 33 wherein said granting unit grants signals for issuing instructions to a predetermined number of instructions based on a plurality of criteria including a time sequence criteria.

36. The microprocessor of claim 31 wherein said dependency unit includes means for resetting elements of entries in response to the signals for issuing instructions.

37. The microprocessor of claim 31 wherein said elements at a same position in the entries are coupled and the coupled elements are manipulated substantially at the same time of issuance of instruction.